EXAMINER'S AMENDMENT

1.   An examiner's amendment to the record appears below. Should the changes and/or

additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR

1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the

payment of the issue fee.

        Authorization for this examiner's amendment was given in a telephone interview with

Mr. Ken Lembke Reg. No. 44,866 on 07/20/2010.

        The application has been amended as follows:

        1. (Currently Amended) A system for providing a floating point product, comprising:

        an analyzer circuit configured to determine a first status of a first floating point operand

and a second status of a second floating point operand based upon data within the first floating

point operand and data within the second floating point operand respectively; wherein the

analyzer circuit comprises:

                a first group of comparators that generate asserted signals responsive to bits in an

        exponent field of the first and second floating point operands;

                a second group of comparators that generate asserted signals responsive to bits of

        a first portion of a fraction field of the first and second floating point operands; and

                a third group of comparators that generate asserted signals responsive to bits of a

        second portion of the fraction field of the first and second floating point operands; and

        a results circuit coupled to the analyzer circuit and configured to assert a resulting

floating point operand containing the product of the first floating point operand and the second

floating point operand and a resulting status embedded within the resulting floating point

operand, wherein each of the first floating point operand, second floating point operand and

resulting floating point operand comprises a sign bit, an exponent field and a fraction field, and

wherein at least one of the five lowest order bits of the fraction field of one of the first floating

point operand, second floating point operand and resulting floating point operand comprises at

least one status flag.

        15. (Currently Amended) A method for providing a floating point product, comprising:

        determining, in an analyzer circuit, a first status of a first floating point operand and a

second status of a second floating point operand based upon data within the first floating point

operand and data within the second floating point operand respectively; wherein the analyzer

circuit comprises:

                a first group of comparators that generate asserted signals responsive to bits in an

        exponent field of the first and second floating point operands;

                a second group of comparators that generate asserted signals responsive to bits of

        a first portion of a fraction field of the first and second floating point operands; and

        a third group of comparators that generate asserted signals responsive to bits of a second

portion of the fraction field of the first and second floating point operands; and

        asserting, in a results circuit, a resulting floating point operand containing the product of

the first floating point operand and the second floating point operand and a resulting status

embedded within the resulting floating point operand, wherein each of the first floating point

operand, second floating point operand and resulting floating point operand comprises a sign bit,

an exponent field and a fraction field, and wherein at least some of the next lowest order bits

after the five lowest order bits of the fraction field encode additional information in relation to

the first, second and resulting statuses.

      46-53. (Canceled)

2.   Claims 28-40 and 46-53 are canceled.

3.   Claims 1-27 and 41-45 are allowed.

      Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Chat C. Do whose telephone number is (571)272-3721. The

examiner can normally be reached on Tue-Fri 7:00AM to 5:30PM.

      If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

      Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

July 26, 2010